L Number	Hits	Search Text	DB	Time stamp
1	4836700	branch victim second	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/24 08:56
2	3710424	cache table storage memory	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/24 08:57
3	2313589	level multilevel	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/24 08:57
4	22900	(branch victim second) with (cache table storage memory) with (level multilevel)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/24 08:53
5	6302	L4.ab.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/24 08:53
6	33	L4.ab. same (decoder instruction)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/24 08:54
7	1880	((branch victim second) with (cache table storage memory) with (level multilevel)) same (decoder instruction)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/24 08:54
8	557890	(branch victim second).ab.	USPAT; US-PGPUB	2004/05/24 08:55
9	259978	(cache table storage memory).ab.	USPAT; US-PGPUB	2004/05/24 08:55
10	129819	(level multilevel).ab.	USPAT; US-PGPUB	2004/05/24 08:56
11	1195	(((branch victim second).ab.) with ((cache table storage memory).ab.)) with ((level multilevel).ab.)	USPAT; US-PGPUB	2004/05/24 08:56
12	93	((((branch victim second).ab.) with ((cache table storage memory).ab.)) with ((level multilevel).ab.)) same (decoder instruction)	USPAT; US-PGPUB	2004/05/24 08:56
13	2009221	branch victim second	EPO; JPO; DERWENT; IBM_TDB	2004/05/24 08:57
14	1964323	cache table storage memory	EPO; JPO; DERWENT; IBM_TDB	2004/05/24 08:57
15	859687	level multilevel	EPO; JPO; DERWENT; IBM_TDB	2004/05/24 08:57
16	3547	(branch victim second) with (cache table storage memory) with (level multilevel)	EPO; JPO; DERWENT; IBM_TDB	2004/05/24 08:57
17	203	((branch victim second) with (cache table storage memory) with (level multilevel)) same (decoder instruction)	EPO; JPO; DERWENT; IBM_TDB	2004/05/24 08:57

L Number	Hits	Search Text	DB	Time stamp
1	1	6141748.pn.	USPAT	2004/05/24 10:35
2	2	6141748.uref.	USPAT	2004/05/24 10:35
3	1	5995749.pn.	USPAT	2004/05/24 10:36
4	7	5995749.uref.	USPAT	2004/05/24 10:37

L Number	Hits	Search Text	DB	Time stamp
20	6	(branch adj marker) adj (bit or bits)	USPAT; US-PGPUB	2004/05/24 11:14
21	0	end adj adjustment adj (bit or bits)	USPAT; US-PGPUB	2004/05/24 11:14
22	0	end adj adjustment adj bit	USPAT; US-PGPUB	2004/05/24 11:15
23	0	end adj adjustment adj bits	USPAT; US-PGPUB	2004/05/24 11:16
24	0	"end adjustment bits"	USPAT; US-PGPUB	2004/05/24 11:16
25	0	"end adjustment bit"	USPAT; US-PGPUB	2004/05/24 11:20
27	1	6055630.pn.	USPAT; US-PGPUB	2004/05/24 11:21
26	1	5758142.pn.	USPAT; US-PGPUB	2004/05/24 11:21

L Number	Hits	Search Text	DB	Time stamp
1	1	4200927.pn.	USPAT; US-PGPUB	2004/05/24 15:26

L Number	Hits	Search Text	DB	Time stamp
1	1	5423011.pn.	USPAT; US-PGPUB; IBM_TDB	2004/05/24 16:07
2	1	"history overflow mechanism".ti.	USPAT; US-PGPUB; IBM_TDB	2004/05/24 16:08

CiteSeer Find: Combining Branch Predictors Documents Citations

Searching for **PHRASE combining branch predictors**.
Restrict to: Header Title Order by: Expected citations Hubs Usage Date Try: Amazon B&N Google (RI) Google (Web) CSB DBLP
4 documents found. **Order: number of citations.**

Combining Branch Predictors - McFarling (1993) (Correct) (165 citations)
J U N E 1 9 9 3 WRL Technical Note TN-36 **Combining Branch Predictors** Scott McFarling d i g i t a l Western
www.ee.lsu.edu/tca/mcf.pdf

Branch Classification: a New Mechanism for Improving Branch.. - Chang (1994) (Correct) (34 citations)
paper, we introduce a new method for **combining branch predictors**. Branches are partitioned into
www.eecs.umich.edu/HPS/pub/class_micro27.ps

Branch Prediction and Simultaneous Multithreading - Hily, Seznec (1996) (Correct) (6 citations)
prediction while McFarling proposed **combining branch predictors** [McF93]Branch prediction strategies
ftp.inria.fr/INRIA/publication/publi-ps-gz/RR/RR-2843.ps.gz

Branch Prediction and Multithreading (V2) - Hily, Seznec (1996) (Correct)
prediction while McFarling proposed **combining branch predictors** [McF93]Branch-prediction strategies
ftp.irisa.fr/techreports/1996/PI-997.ps.gz

Try your query at: Amazon Barnes & Noble Google (RI) Google (Web) CSB DBLP

Terms used
Alternative Implementations of Two Level Adaptive Branch Prediction

Found **30** of **134,837**

Sort results by: relevance
Display results: expanded form
Save results to a Binder
Search Tips
Open results in a new window

Try an Advanced Search
Try this search in The ACM Guide

Results 1 - 20 of 30 Result page: **1** 2 next

Relevance scale

1 Alternative implementations of two-level adaptive branch prediction
Tse-Yu Yeh, Yale N. Patt
April 1992 **ACM SIGARCH Computer Architecture News , Proceedings of the 19th annual international symposium on Computer architecture**, Volume 20 Issue 2
Full text available: pdf(1.29 MB) Additional Information: full citation, abstract, references, citings, index terms

As the issue rate and depth of pipelining of high performance Superscalar processors increase, the importance of an excellent branch predictor becomes more vital to delivering the potential performance of a wide-issue, deep pipelined microarchitecture. We propose a new dynamic branch predictor (Two-Level Adaptive Branch Prediction) that achieves substantially higher accuracy than any other scheme reported in the literature. The mechanism uses two levels of branch history information to make ...

2 Alternative implementations of two-level adaptive branch prediction
Tse-Yu Yeh, Yale N. Patt
August 1998 **25 years of the international symposia on Computer architecture (selected papers)**
Full text available: pdf(1.39 MB) Additional Information: full citation, references, index terms

3 A comparison of dynamic branch predictors that use two levels of branch history
Tse-Yu Yeh, Yale N. Patt
May 1993 **ACM SIGARCH Computer Architecture News , Proceedings of the 20th annual international symposium on Computer architecture**, Volume 21 Issue 2
Full text available: pdf(987.31 KB) Additional Information: full citation, abstract, references, citings, index terms

Recent attention to speculative execution as a mechanism for increasing performance of single instruction streams has demanded substantially better branch prediction than what has been previously available. We [1,2] and Pan, So, and Rahmen [4] have both proposed variations of the same aggressive dynamic branch predictor for handling those needs. We call the basic model Two-Level Adaptive Branch Prediction; Pan, So, and Rahmeh call it Correlation Branch Prediction. In this paper, we adopt th ...

4 Increasing the instruction fetch rate via multiple branch prediction and a branch address cache
Tse-Yu Yeh, Deborah T. Marr, Yale N. Patt
August 1993 **Proceedings of the 7th international conference on Supercomputing**
Full text available: pdf(1.13 MB) Additional Information: full citation, references, citings, index terms, review

5 Retrospective: alternative implementations of two-level adaptive training branch prediction

Tse-Yu Yeh, Yale N. Patt

August 1998 **25 years of the international symposia on Computer architecture (selected papers)**

Full text available: pdf(220.18 KB) Additional Information: full citation, references, index terms

6 The impact of unresolved branches on branch prediction scheme performance

A. R. Talcott, W. Yamamoto, M. J. Serrano, R. C. Wood, M. Nemirovsky

April 1994 **ACM SIGARCH Computer Architecture News , Proceedings of the 21ST annual international symposium on Computer architecture**, Volume 22 Issue 2

Full text available: pdf(871.86 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper, we examine the benefits of the early resolution of branch instructions and the impact of unresolved branches on history-based branch prediction schemes by using two new metrics that are more revealing than branch prediction accuracy alone. We first briefly review a number of branch prediction schemes and introduce two new branch prediction scheme performance metrics. We then utilize these metrics to gauge the improvement in branch prediction scheme performance when only the outcom ...

7 Completion time multiple branch prediction for enhancing trace cache performance

Ryan Rakvic, Bryan Black, John Paul Shen

May 2000 **ACM SIGARCH Computer Architecture News , Proceedings of the 27th annual international symposium on Computer architecture**, Volume 28 Issue 2

Full text available: pdf(155.82 KB) Additional Information: full citation, abstract, references, citings, index terms

The need for multiple branch prediction is inherent to wide instruction fetching. This paper presents a completion time multiple branch predictor called the Tree-based Multiple Branch Predictor (TMP) that builds on previous single branch prediction techniques. It employs a tree structure of branch predictors, or tree-node predictors, and achieves accurate multiple branch prediction by leveraging the high accuracies of the individual branch predictors. A highly-efficient TMP design u ...

8 Dynamic removal of redundant computations

Carlos Molina, Antonio González, Jordi Tubella

May 1999 **Proceedings of the 13th international conference on Supercomputing**

Full text available: pdf(1.09 MB) Additional Information: full citation, references, citings, index terms

Keywords: data-value reuse, instruction-level parallelism, instruction-level reuse

9 Predicting indirect branches via data compression

John Kalamatianos, David R. Kaeli

November 1998 **Proceedings of the 31st annual ACM/IEEE international symposium on Microarchitecture**

Full text available: pdf(1.24 MB) Additional Information: full citation, references, citings, index terms

10 Load latency tolerance in dynamically scheduled processors

Srikanth T. Srinivasan, Alvin R. Lebeck

November 1998 **Proceedings of the 31st annual ACM/IEEE international symposium on**

Microarchitecture

Full text available: pdf(3.25 MB) Additional Information: full citation, references, citings, index terms

11 The effect of instruction fetch bandwidth on value prediction

Freddy Gabbay, Avi Mendelson

April 1998 **ACM SIGARCH Computer Architecture News , Proceedings of the 25th annual international symposium on Computer architecture**, Volume 26 Issue 3

Full text available: pdf(1.32 MB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Value prediction attempts to eliminate true-data dependencies by dynamically predicting the outcome values of instructions and executing true-data dependent instructions based on that prediction. In this paper we attempt to understand the limitations of using this paradigm in realistic machines. We show that the instruction-fetch bandwidth and the issue rate have a very significant impact on the efficiency of value prediction. In addition, we study how recent techniques to improve the instructio ...

12 Kin: a high performance asynchronous processor architecture

Rakefet Kol, Ran Ginosar

July 1998 **Proceedings of the 12th international conference on Supercomputing**

Full text available: pdf(1.03 MB) Additional Information: full citation, references, citings, index terms

Keywords: asynchronous architecture, avid execution, dynamic instance tag, multi-execution, pruning

13 Using prediction to accelerate coherence protocols

Shubhendu S. Mukherjee, Mark D. Hill

April 1998 **ACM SIGARCH Computer Architecture News , Proceedings of the 25th annual international symposium on Computer architecture**, Volume 26 Issue 3

Full text available: pdf(1.71 MB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Most large shared-memory multiprocessors use directory protocols to keep per-processor caches coherent. Some memory references in such systems, however, suffer long latencies for misses to remotely-cached blocks. To ameliorate this latency, researchers have augmented standard coherence protocols with optimizations for specific sharing patterns, such as read-modify-write, producer-consumer, and migratory sharing. This paper seeks to replace these directed solutions with general prediction logic t ...

14 Branch prediction based on universal data compression algorithms

Eitan Federovsky, Meir Feder, Sholomo Weiss

April 1998 **ACM SIGARCH Computer Architecture News , Proceedings of the 25th annual international symposium on Computer architecture**, Volume 26 Issue 3

Full text available: pdf(987.72 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Data compression and prediction are closely related. Thus prediction methods based on data compression algorithms have been suggested for the branch prediction problem. In this work we consider two universal compression algorithms: prediction by partial matching (PPM), and a recently developed method, context tree weighting (CTW). We describe the prediction algorithms induced by these methods. We also suggest adaptive algorithms --- variations of the basic methods that attempt to fit limited mem ...

15 Can program profiling support value prediction?

Freddy Gabbay, Avi Mendelson
December 1997 **Proceedings of the 30th annual ACM/IEEE international symposium on Microarchitecture**

Full text available: pdf(1.41 MB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

This paper explores the possibility of using program profiling to enhance the efficiency of value prediction. Value prediction attempts to eliminate true-data dependencies by predicting the outcome values of instructions at run-time and executing true-data dependent instructions based on that prediction. So far, all published papers in this area have examined hardware-only value prediction mechanisms. In order to enhance the efficiency of value prediction, it is proposed to employ program profil ...

Keywords: Value-prediction, instruction-level parallelism, speculative execution.

16 Control flow prediction with tree-like subgraphs for superscalar processors
Simonjit Dutta, Manoj Franklin
December 1995 **Proceedings of the 28th annual international symposium on Microarchitecture**

Full text available: pdf(660.81 KB) Additional Information: full citation, references, citings, index terms

17 A fill-unit approach to multiple instruction issue
Manoj Franklin, Mark Smotherman
November 1994 **Proceedings of the 27th annual international symposium on Microarchitecture**

Full text available: pdf(992.94 KB) Additional Information: full citation, abstract, references, citings, index terms

Multiple issue of instructions occurs in superscalar and VLIW machines. This paper investigates a third type of machine design, which combines the advantages of code compatibility as in superscalars and the absence of complex dependency-checking logic from the decoder as in VLIW. In this design, a stream of scalar instructions is executed by the hardware and is simultaneously compacted into VLIW-type instructions, which are then stored in a structure called a shadow cache. When a shadow cac ...

Keywords: VLIW, instruction-level parallelism, multiple operation issue, superscalar

18 Superscalar microarchitecture: Exploiting data-width locality to increase superscalar execution bandwidth
Gabriel H. Loh
November 2002 **Proceedings of the 35th annual ACM/IEEE international symposium on Microarchitecture**

Full text available: pdf(1.13 MB) Publisher Site Additional Information: full citation, abstract, references, index terms

In a 64-bit processor, many of the data values actually used in computations require much narrower data-widths. In this study, we demonstrate that instruction data-widths exhibit very strong temporal locality and describe mechanisms to accurately predict data-widths.To exploit the predictability of data-widths, we propose a Multi-Bit-Width (MBW) microarchitecture which, when the opportunity arises, takes the wires normally used to route the operands and bypass the result of a 64-bit instruction, ...

19 Using hybrid branch predictors to improve branch prediction accuracy in the presence of context switches
Marius Evers, Po-Yung Chang, Yale N. Patt
May 1996 **ACM SIGARCH Computer Architecture News , Proceedings of the 23rd**

annual international symposium on Computer architecture, Volume 24 Issue 2

Full text available: pdf(916.36 KB) Additional Information: full citation, abstract, references, citings, index terms

Pipeline stalls due to conditional branches represent one of the most significant impediments to realizing the performance potential of deeply pipelined, superscalar processors. Many branch predictors have been proposed to help alleviate this problem, including the Two-Level Adaptive Branch Predictor, and more recently, two-component hybrid branch predictors.In a less idealized environment, such as a time-shared system, code of interest involves context switches. Context switches, even at fairly ...

Keywords: branch prediction, context switch, speculative execution, superscalar

20 Correlation and aliasing in dynamic branch predictors

Stuart Sechrest, Chih-Chieh Lee, Trevor Mudge

May 1996 **ACM SIGARCH Computer Architecture News , Proceedings of the 23rd annual international symposium on Computer architecture**, Volume 24 Issue 2

Full text available: pdf(1.60 MB) Additional Information: full citation, abstract, references, citings, index terms

Previous branch prediction studies have relied primarily upon the SPECint89 and SPECint92 benchmarks for evaluation. Most of these benchmarks exercise a very small amount of code. As a consequence, the resources required by these schemes for accurate predictions of larger programs have not been clear. Moreover, many of these studies have simulated a very limited number of configurations. Here we report on simulations of a variety of branch prediction schemes using a set of relatively large bench ...

Results 1 - 20 of 30 Result page: **1** 2 next